24dB Range, 1dB Step Size Programmable
VGA

## Preliminary Technical Data

## FEATURES

-4 to 20dB Gain Range<br>$\mathbf{1 d B}$ Step Size $\pm 0.2 \mathrm{~dB}$<br>Differential input and output<br>$150 \Omega$ Differential Input<br>Open Collector Differential Output<br>8dB noise figure @ maximum gain<br>OIP3 of $\sim 50 \mathrm{dBm}$ at 140 MHz<br>-3 dB bandwidth of 690 MHz<br>Parallel 5-bit Control Interface<br>Wide input dynamic range<br>Power-down feature<br>Single 5V Supply Operation<br>24 Lead LFCSP $4 \times 4$ mm Package<br>APPLICATIONS<br>Differential ADC drivers<br>High IF Sampling Receivers<br>High Output Power IF Amplification<br>Instrumentation

## GENERAL DESCRIPTION

The AD8375 is a digitally controlled, variable gain wide bandwidth amplifier that provides precise gain control, high IP3 and low noise figure. The excellent distortion performance and high signal bandwidth makes the AD8375 an excellent gain control device for a variety of receiver applications.

For wide input dynamic range applications, the AD8375 provides a broad 24 dB gain range with 1 dB resolution. The gain is adjusted through a 5 -pin control interface and can be driven using standard TTL levels. The open-collector outputs provide a flexible interface, allowing the overall signal gain to be set by the loading resistance. The AD8375 offers a maximum transconductance gain of $67 \mathrm{~m} \Omega^{-1} \mathrm{~s}$, resulting in a signal gain of 20 dB when driving a $150-\mathrm{Ohm}$ load. The maximum signal gain increases to $\sim 24 \mathrm{~dB}$ when driving a 250 -Ohm differential load.


Using a high speed SiGe process and incorporating proprietary distortion cancellation techniques, the AD8375 achieves 50 dBm output IP3 at 140 MHz .

The AD8375 is powered on by applying the appropriate logic level to the PWUP pin. The quiescent current of the AD8375 is typically 130 mA . When powered down, the AD8375 consumes less than 5 mA and offers excellent input to output isolation. The gain setting is preserved when powered down.

Fabricated on an ADI's high speed SiGe process, the AD8375 provides precise gain adjustment capabilities with good distortion performance. The AD8375 amplifier comes in a compact, thermally enhanced $4 \times 4 \mathrm{~mm}$ 24-lead LFCSP package and operates over the temperature range of $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$.

## SPECIFICATIONS

$\mathrm{V}_{\mathrm{S}}=5 \mathrm{~V}, \mathrm{~T}=25^{\circ} \mathrm{C}, \mathrm{Z}_{\mathrm{S}}=\mathrm{Z}_{\mathrm{L}}=150 \Omega$ at $100 \mathrm{MHz}, 2 \mathrm{~V}$ p-p differential output unless otherwise noted.
Table 1.

| Parameter | Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DYNAMIC PERFORMANCE <br> -3 dB Bandwidth <br> Slew Rate | $\mathrm{V}_{\text {OUT }}<2 \mathrm{~V}$ p-p (5.2dBm) |  | $\begin{aligned} & 690 \\ & \text { TBD } \end{aligned}$ |  | MHz <br> V/nsec |
| INPUT STAGE <br> Maximum Input Swing Differential Input Resistance Common-Mode Input Voltage CMRR | Pins VIN+ and VIN- <br> For linear operation $\left(\mathrm{A}_{\mathrm{v}}=0 \mathrm{~dB}\right)$ <br> Differential <br> Gain Code $=00000$ |  | $\begin{aligned} & \text { TBD } \\ & 150 \\ & 2 \\ & \text { TBD } \end{aligned}$ |  | $\begin{aligned} & \text { Vp-p } \\ & \Omega \\ & V \\ & d B \end{aligned}$ |
| GAIN <br> Amplifier Transconductance <br> Maximum Voltage Gain <br> Minimum Voltage Gain <br> Gain Step Size <br> Gain Flatness <br> Gain Temperature Sensitivity <br> Gain Step Response | Gain Code $=00000$ <br> Gain Code $\geq 11000$ <br> From Gain Code 00000 to 11000 <br> Gain Code $=00000$ over 20\% fractional <br> bandwidth for $\mathrm{fc}_{\mathrm{c}}<200 \mathrm{MHz}$ <br> Gain Code $=00000$ <br> For $\mathrm{V}_{\mathbb{I}}=0.2 \mathrm{~V}$, Gain Code 10100 to 00000 | $\begin{aligned} & 0.58 \\ & -5.5 \\ & 0.8 \end{aligned}$ | 0.067 20 -4 1.0 TBD TBD TBD | $\begin{aligned} & 0.076 \\ & -2.5 \\ & 1.2 \end{aligned}$ | $\Omega^{-1}$ <br> dB <br> dB <br> dB <br> dB <br> $\mathrm{mdB} /{ }^{\circ} \mathrm{C}$ <br> ns |
| OUTPUT STAGE <br> Output Voltage Swing <br> Output impedance | Pins OUT+ and OUT- <br> At P1dB, Gain Code $=00000$ <br> Differential |  | $\begin{aligned} & 10 \\ & 5 \mathrm{k} / / 1 \end{aligned}$ |  | $\begin{aligned} & \text { Vp-p } \\ & \Omega / p F \end{aligned}$ |
| NOISE/HARMONIC PERFORMANCE <br> 46 MHz <br> Noise Figure <br> Second Harmonic <br> Third Harmonic <br> Output IP3 <br> Output 1 dB Compression Point | Gain Code $=00000$ $\begin{aligned} & \mathrm{V}_{\text {out }}=2 \mathrm{~V} \text { p-p } \\ & \mathrm{V}_{\text {out }}=2 \mathrm{~V} \text { p-p } \end{aligned}$ <br> 2 MHz spacing, +3 dBm per tone |  | $\begin{aligned} & 8.5 \\ & -94 \\ & -92 \\ & 50 \\ & 19 \end{aligned}$ |  | dB <br> dBc <br> dBc <br> dBm <br> dBm |
| 70 MHz <br> Noise Figure <br> Second Harmonic <br> Third Harmonic <br> Output IP3 <br> Output 1 dB Compression Point | $\text { Gain Code }=00000$ $\begin{aligned} & V_{\text {out }}=2 \mathrm{~V} p-\mathrm{p} \\ & \mathrm{~V}_{\text {out }}=2 \mathrm{Vp}-\mathrm{p} \end{aligned}$ <br> 2 MHz spacing, +3 dBm per tone |  | $\begin{aligned} & 8.5 \\ & -94 \\ & -92 \\ & 50 \\ & 19 \end{aligned}$ |  | dB <br> dBc <br> dBc <br> dBm <br> dBm |
| 140 MHz <br> Noise Figure <br> Second Harmonic <br> Third Harmonic <br> Output IP3 <br> Output 1 dB Compression Point | $\text { Gain Code }=00000$ $\begin{aligned} & V_{\text {out }}=2 \mathrm{~V} p-\mathrm{p} \\ & \mathrm{~V}_{\text {out }}=2 \mathrm{Vp}-\mathrm{p} \end{aligned}$ <br> 2 MHz spacing, +3 dBm per tone |  | $\begin{aligned} & 8.5 \\ & -86 \\ & -91 \\ & 50 \\ & 19 \end{aligned}$ |  | dB <br> dBc <br> dBc <br> dBm <br> dBm |


| Parameter | Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 200 MHz <br> Noise Figure <br> Second Harmonic <br> Third Harmonic <br> Output IP3 <br> Output 1 dB Compression Point | $\text { Gain Code }=00000$ $\begin{aligned} & \text { Vout }=2 \mathrm{~V} \text { p-p } \\ & \text { Vout }=2 \mathrm{Vp} \text { p-p } \end{aligned}$ <br> 2 MHz spacing, +3 dBm per tone |  | $\begin{aligned} & 8.5 \\ & -85 \\ & -88 \\ & 50 \\ & 18 \end{aligned}$ |  | dB <br> dBc <br> dBc <br> dBm <br> dBm |
| POWER-INTERFACE <br> Supply Voltage <br> Quiescent Current per Channel <br> vs. Temperature <br> Power Down Current vs. Temperature | thermal connection made to exposed paddle under device $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+85^{\circ} \mathrm{C}$ <br> PWUP Low $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+85^{\circ} \mathrm{C}$ | 4.5 | 130 3 | 5.5 <br> 140 <br> 165 <br> TBD | V <br> mA <br> mA <br> mA <br> mA |
| ENABLE INTERFACE <br> Enable Threshold <br> PWUP Input Bias Current | Pin PWUP <br> Minimum voltage to enable the device |  | 0.5 | 1.6 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{nA} \end{aligned}$ |
| GAIN CONTROL INTERFACE <br> $\mathrm{V}_{\mathrm{H}}$ <br> VII <br> Maximum Input Bias Current | Pins A0, A1, A2, A3, A4 <br> Minimum voltage for a logic high Maximum voltage for a logic low | 1.6 | 900 | 0.8 |  |

Table 2. Gain-Code versus Voltage Gain Look-Up Table

| 5-Bit Binary Gain Code | Voltage Gain (dB) | 5-Bit Binary Gain Code | Voltage Gain (dB) |
| :---: | :---: | :---: | :---: |
| 00000 | 20 | 01101 | 7 |
| 00001 | 19 | 01110 | 6 |
| 00010 | 18 | 01111 | 5 |
| 00011 | 17 | 10000 | 4 |
| 00100 | 16 | 10001 | 3 |
| 00101 | 15 | 10010 | 2 |
| 00110 | 14 | 10011 | 1 |
| 00111 | 13 | 10100 | 0 |
| 01000 | 12 | 10101 | -1 |
| 01001 | 11 | 10110 | -2 |
| 01010 | 10 | 10111 | -3 |
| 01011 | 9 | 11000 | -4 |
| 01100 | 8 | $>11000$ | -4 |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Rating |
| :--- | :--- |
| Supply Voltage, $\mathrm{V}_{\text {POS }}$ | 5.5 V |
| PWUP, A0, $\mathrm{A} 1, \mathrm{~A} 2, \mathrm{~A} 3, \mathrm{~A} 4$ | -0.6 to $(\mathrm{V}$ POS $+0.6 \mathrm{~V})$ |
| Input Voltage, $\mathrm{V}_{\mathrm{IN}+}, \mathrm{V}_{\text {IN }}$ | -0.6 to +3.1 V |
| Internal Power Dissipation | TBD mW |
| $\theta_{\mathrm{JA}}$ (Exposed paddle soldered down) | $\mathrm{TBD}^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\theta_{\mathrm{JA}}$ (Exposed paddle not soldered down) | $\mathrm{TBD}^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\theta_{\mathrm{JC}}($ At exposed paddle) | $\mathrm{TBD}^{\circ} \mathrm{C} / \mathrm{W}$ |
| Maximum Junction Temperature | $\mathrm{TBD}^{\circ} \mathrm{C}$ |
| Operating Temperature Range | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Lead Temperature Range | $\mathrm{TBD}^{\circ} \mathrm{C}$ |
| (Soldering 60 sec) |  |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS


Table 3. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
| :--- | :--- | :--- |
| 1 | VCOM | Common Mode Pin. Typically bypassed to ground using external capacitor. |
| 2 | VIN+ | Voltage Input Positive. |
| 3 | VIN- | Voltage Input Negative. |
| 4 | A4 | The Most Significant Bit (MSB) for the 5-bit Gain Control Interface. |
| 5 | A3 | MSB-1 for the Gain Control Interface. |
| 6 | A2 | MSB-2 for the Gain Control Interface. |
| 7 | A1 | LSB+1 for the Gain Control Interface. |
| 8 | AO | The Least Significant Bit (LSB) for the 5-bit Gain Control Interface. |
| $9,10,12,13$, | VPOS | Positive Supply Pins. Should be bypassed to Ground using suitable bypass capacitor. |
| 23 |  |  |
| $11,14,20$, | COMM | Device Common (DC Ground). |
| $21,22,24$ |  |  |
| 15,17 | VOUT+ | Positive Ouptut Pins (Open Collector). Require DC bias of +5 V nominal. |
| 16,18 | VOUT- | Negative Ouptut Pins (Open Collector). Require DC bias of +5 V nominal. |
| 19 | PWUP | Chip Enable Pin. |

## OUTLINE DIMENSIONS

## 24-Lead Frame Chip Scale Package [LFCSP] <br> 4 mm x 4 mm Body

(CP-24)
Dimensions shown in millimeters


Figure2. 24-Lead LFCSP)

## ORDERING GUIDE

| Model | Temperature | Package Description | Package Option |
| :--- | :--- | :--- | :--- |
| AD8375ACPZ-WP | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | Waffle Pack, 24 Lead Frame Chip Scale <br> Package <br> $7 "$ Reel, 24 Lead Frame Chip Scale Package <br> AD8375ACPZ-REEL7 | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |

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